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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,265	04/02/2004	Fouad A. Faour	10030219-1	1790
7590	12/28/2005		EXAMINER	
AGILENT TECHNOLOGIES, INC.			PRUCHNIC, STANLEY J	
Legal Department, DL429			ART UNIT	PAPER NUMBER
Intellectual Property Administration				
P.O. Box 7599			2859	
Loveland, CO 80537-0599			DATE MAILED: 12/28/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/817,265	FAOUR ET AL.	
	Examiner	Art Unit	
	Stanley J. Pruchnic, Jr.	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 03 October 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 03 October 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see "REMARKS/ARGUMENTS", filed 03 October 2005, with respect to the rejection(s) of claim(s) **1-3 and 7-17** under 35 U.S.C. 102(b) have been fully considered and are persuasive. Applicant's argument, to summarize, is that the power supply, as disclosed by DAVIDSON, is not a part of the integrated circuit as claimed by Applicant in independent claims 1 and 7.
2. In response to applicant's arguments, the recitation in the preamble "An integrated circuit" has been given sufficient patentable weight to require the constant current source to be a component of the integrated circuit. The preamble has been accorded patentable weight because all the claimed elements are considered to be formed on an integrated circuit in order that the integrated circuit "comprises" the claimed elements. The preamble does not merely recite the purpose of a process or the intended use of a structure, and the body of the claim does depend on the preamble for completeness, the structural limitations having been considered not able to stand alone, as claimed by Applicant. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).
3. Applicant's arguments with respect to the rejection(s) of claim(s) **4 and 19; 5 and 20 and 18** under 35 U.S.C. 103(a) have been fully considered and are persuasive as described above with regard to Claims 1-3 and 7-17.
4. Applicant's arguments filed 03 October 2005, with respect to the rejection(s) of claim(s) **6**, have been fully considered but they are not persuasive. Applicant's argument suggesting that a power supply is not a part of the integrated circuit is not persuasive, since a constant current will be supplied "on-board the integrated circuit" in the normal practice of the method as taught by **TANAKA** and **NISHIZAWA**, the location of the power supply not affecting the method in a manipulative sense, and not being positively claimed.

Drawings

5. The corrected or substitute drawings (sheet 1, now including a legend indicating it is -- Prior Art --) were received on 03 October 2005. The examiner has previously approved this drawing.
6. The corrected or substitute drawings (sheet 2, re-numbering the drawing to now be --Fig. 3--) were received on 18 August 2004. The examiner has previously approved this drawing.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 1-3, 5, 7-17 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5639163 A (Davidson; Evan Ezra et al., hereinafter DAVIDSON) in view of US 6554469 B1 (Thomson; David et al., hereinafter THOMSON).

DAVIDSON discloses or suggests an integrated circuit as claimed by Applicant in **Claims 1-3, 5, 7-17 and 20**, comprising:

Regarding **Claim 1**: DAVIDSON discloses an integrated circuit comprising

a number of pads;
a constant current source (power supply; Fig. 2) to provide a current I1;
a thermal diode D1 that receives said current I1, said thermal diode being
coupled between first C4A and second (Ground pad, not explicitly shown) ones of said
pads;
an analog to digital converter 36 to
i) receive a forward bias voltage (V1) of the thermal diode D1 (Col. 2, Lines 49-
51), and
ii) output (to microprocessor 37; Col. 3, Lines 61-64) a digital representation of
the forward bias voltage (V2 -V1).

Regarding **Claim 7**: DAVIDSON discloses an integrated circuit comprising
a constant current source to provide first and second currents of different
magnitudes;

first D1 and second D2 thermal diodes that respectively receive said first I1 and
second I2 currents;

a comparator 32 (Fig. 3) to receive forward bias voltages of each of the thermal
diodes, to compare the forward bias voltages, and to output a voltage difference
indicative of a temperature of the integrated circuit.

Further regarding **Claims 2-3 and 17**, DAVIDSON discloses logic 37 to receive
the digital representation of the forward bias voltage and calculate a temperature of the
integrated circuit (Col. 3, Lines 50-52; and Col. 4, Lines 1-4), wherein said logic
comprises a temperature look-up table 39 as claimed by Applicant in **Claims 3 and 17**.

Further regarding **Claims 5 and 20**, DAVIDSON discloses a third one of said
pads is provided to receive a reference current, said third pad C4B being coupled to an
input of said constant current source as claimed by Applicant in Claim 5; further
comprising a pad to receive a reference current, said pad being coupled to an input of
said constant current source as claimed by Applicant in Claim 20.

Further regarding **Claims 8-10 and 16**: DAVIDSON discloses the thermal diodes
are positioned adjacent one another (Col. 2, Lines 45-49) as claimed by Applicant in
Claim 8, and the first and second currents have a known relationship as claimed by

Applicant in **Claims 9 and 16**, and further regarding **Claim 10**, the second current I2 is an integer multiple of the first current I1 (Col. 3, Lines 6-15; e.g., a ratio of 100:1).

Further regarding **Claim 11**: DAVIDSON discloses the comparator 32 is a differential amplifier.

Further regarding **Claims 12 and 14**, DAVIDSON discloses the integrated circuit further comprising an analog to digital converter 36 to

- i) receive the voltage difference output by the differential amplifier, and
- ii) output a digital representation of the voltage difference.

Further regarding **Claims 13 and 15**, DAVIDSON discloses the integrated circuit further comprising logic 37 to receive the digital representation of the voltage difference and calculate a temperature of the integrated circuit.

DAVIDSON, to summarize, discloses or suggests all the limitations as claimed by Applicant in **Claims 1-3, 5, 7-17 and 20**, as described above, except DAVIDSON's power supply V_p is off the "chip area" as indicated by chip 12 (Fig. 12), therefore is not considered to be a part of the integrated circuit disclosed by DAVIDSON. DAVIDSON as described above, does not explicitly disclose said reference current thereby serving to control the constant current source.

THOMSON discloses a control current provided as a reference current to an input of an "on-chip" constant current source, thereby serving to control the constant current source.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a control current provided as a reference current to an input of an on-chip constant current source, thereby serving to control the constant current source for the fixed resistor controlled source of DAVIDSON in order to make the constant current source adjustable as taught by THOMSON.

10. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over DAVIDSON and THOMSON in view of US 6453218 B1 (Vergis; George, hereinafter VERGIS).

DAVIDSON and THOMSON, to summarize, discloses or suggests all the limitations as claimed by Applicant in Claims 4 and 19, as described above in Paragraph 9 as applied to **Claims 1-3, 5, 7-17 and 20** further including the limitations that the microprocessor 37 has an input that receives the digital representation of the differential input voltage, the digital representation of the voltage difference (between the two forward bias voltages) as claimed by Applicant, and includes a look-up table for converting those values to temperature values, and the microprocessor 37 outputs these values over a suitable bus 41. DAVIDSON discloses that the microprocessor 37 may compare the measured value to a limit and provide an over-temperature output signal to a lead 40 (Col. 3, Line 61 - Col. 4, Line 8).

DAVIDSON as described above, does not explicitly disclose a register to store the digital representation of the forward bias voltage, the digital representation of the voltage difference as claimed by Applicant, said register being readable during normal operation of the integrated circuit as claimed by Applicant.

VERGIS discloses it is known in the art to store the digital representation of a temperature that is based on the forward bias voltage across a diode in a register area 104 (Col. 3, Lines 15-33).

VERGIS further discloses that it is advantageous to store the digital representation of temperature in a register in order to benefit from the ability to periodically store the data as it is measured, but only read it at convenient times that will not interfere with other processor operations (Col. 3, Lines 34-54).

VERGIS is evidence that ordinary workers in the field of temperature measurement in integrated circuits would recognize the benefit of adding a register being readable during normal operation of the integrated circuit as taught by VERGIS for the device of DAVIDSON in order to benefit from not interfering with other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a register being readable during normal operation for the transmitted output signal of DAVIDSON in order to not interfering with

other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted as taught by VERGIS.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **DAVIDSON and THOMSON** in view of US 5195827 A (**AUDY**; Jonathan M. et al.).

DAVIDSON and THOMSON, to summarize, discloses or suggests all the limitations as claimed by Applicant in Claim 18, as described above in Paragraph 9 as applied to **Claims 1-3, 5, 7-17 and 20** further including the limitations of one analog to digital converter 36 receiving the output of comparator 32. DAVIDSON further disclosed that the currents should be precisely controlled by selecting external resistors with precisely known values.

DAVIDSON as described above, does not explicitly disclose one or more analog to digital converters receiving the first and second currents and outputting digital representations of said currents to logic.

AUDY discloses an ammeter 24 and analog to digital converter 38 for providing the current data to the central processor 36.

AUDY is evidence that ordinary workers in the field of semiconductor device temperature sensing would recognize the benefit of using an analog to digital converter as taught by AUDY for the precisely known resistors of DAVIDSON in order to measure the currents for better accuracy without requiring the resistors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute an analog to digital converter for the precise resistors controlling the current of DAVIDSON in order to use multiple excitations and cancel parasitic base and emitter resistances as taught by AUDY.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6890097 B2 (**TANAKA**; Nobue) in view of US 5401099 A (Nishizawa; Hideaki et al., hereinafter **NISHIZAWA**).

TANAKA, to summarize, discloses or suggests all the limitations as claimed by Applicant in Claim 6: a method for measuring a temperature of an integrated circuit, comprising;

coupling (Fig. 14, Col. 19; Step 1403) first 96 and second 98 pads of the integrated circuit to a characterization device (test head 114; Fig. 17; Col. 17, Lines 49-52ff; Col. 18: Line 17-Col. 19, Line 3), said first and second pads being coupled to terminals of a thermal diode 86 of the integrated circuit;

supplying (step 1404) a first current to the thermal diode (80A), via the characterization device, to determine a saturation current of the thermal diode;

disconnecting (after step 1410: "END") the characterization device from the integrated circuit;

during normal operation of the integrated circuit, and on-board the integrated circuit, supplying a constant current to the thermal diode while converting a forward bias voltage of the thermal diode to a digital value; and

using said digital value in conjunction with a digital representation of said saturation current to calculate the temperature of the integrated circuit.

TANAKA as described above, does not explicitly disclose during normal operation of the integrated circuit, and on-board the integrated circuit, supplying a constant current to the thermal diode while converting a forward bias voltage of the thermal diode to a digital value; and

using said digital value in conjunction with a digital representation of said saturation current to calculate the temperature of the integrated circuit.

NISHIZAWA discloses measuring a forward voltage in a main measurement stage after measurement of forward current/voltage characteristics and storing correction values.

NISHIZAWA is evidence that ordinary workers in the field of temperature measurement would recognize the benefit of using stored corrections as taught by **NISHIZAWA** for the calibration of **TANAKA** in order to more accurately measure the temperature.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute supplying a constant current for the supplying of a voltage of TANAKA in order to more accurately measure the temperature as taught by NISHIZAWA.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in a form PTO-892 and not mentioned above disclose related temperature measurement devices and methods.

Previously cited, US 20040071183 A1 (Tesi, Davide et al.) also discloses (Paragraph [0049] a register 5 for storing digital temperature data.

Newly cited documents include related integrated circuits with temperature sensing elements: US 6774653 B2 (Gold; Spencer M. et al.) and US 6674185 B2 (Mizuta; Masaru).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanley J. Pruchnic, Jr., whose telephone number is **(571) 272-2248**. The examiner can normally be reached on weekdays (Monday through Friday), the best hours being from 8:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez (Art Unit 2859) can be reached at **(571) 272-2245**. The Central FAX Number for all official USPTO communications is **571-273-8300**.

15. Any inquiry of a general nature or relating to the status of this application or proceeding may be directed to the official USPTO website at <http://www.uspto.gov> or you may call the **USPTO Call Center** at **800-786-9199** or 703-308-4357. The Technology Center 2800 Customer Service FAX phone number is (703) 872-9317.

The cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources.

Private PAIR provides external customers Internet-based access to patent application status and history information as well as the ability to view the scanned images of each customer's own application file folder(s).

16. For inquiries relating to Patent e-business products and service applications, you may call the *Patent Electronic Business Center (EBC)* at 703-305-3028 or toll free at 866-217-9197 between the hours of 6 a.m. and midnight Monday through Friday EST, or by e-mail at: ebc@uspto.gov. Additional information is available on the Patent EBC Web site at: <http://www.uspto.gov/ebc/index.html>.

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Stanley J. Pruchnic, Jr.
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